# Novel Embedded Computer Architectures for KASSPER

**Matt French**

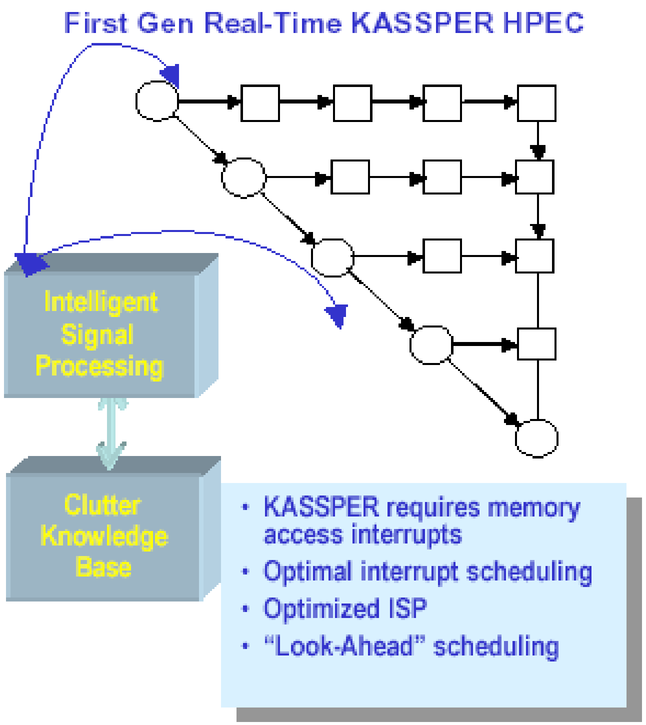
**University of Southern California /Information Sciences Institute**

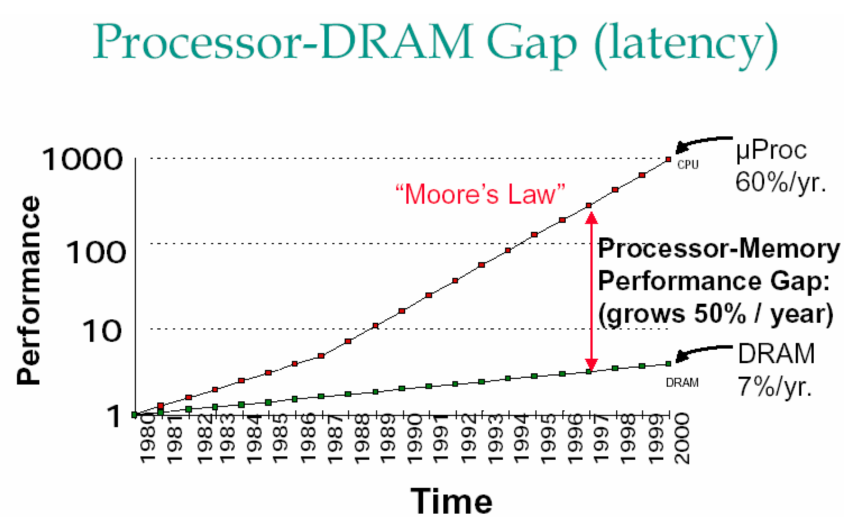
**www.east.isi.edu**

**April 15th, 2003**

# Motivation

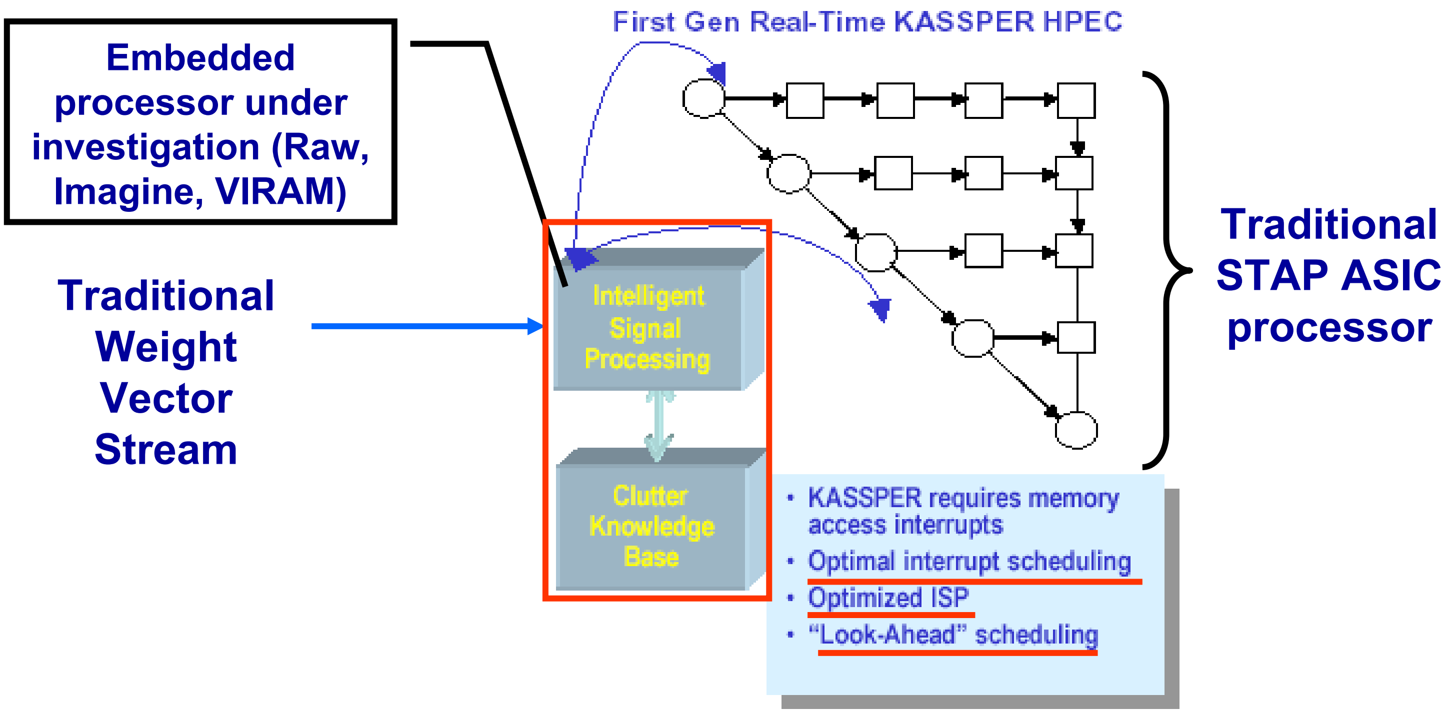
- **KASSPER algorithms blend Knowledge processing with traditional signal processing**
- **Traditional Signal Processing**
  - FLOPs
- **Knowledge Processing**
  - Database Access Rates
  - Large Memory Structures
- **New Set of Computer Architecture Parameters Stressed**
  - Memory Latency
  - I/O Throughput
  - Multi-threaded Application Performance
  - Data Locality



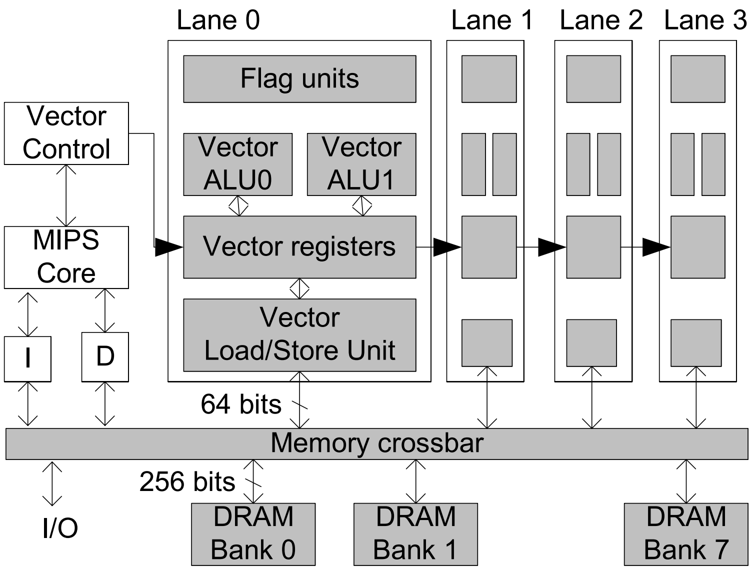
# Research Goals

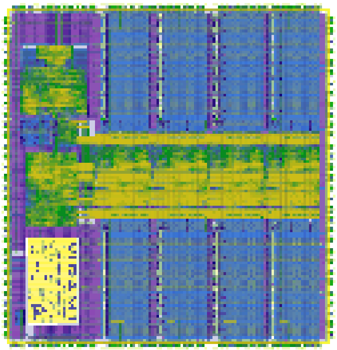
- Identify emerging embedded computing technology capable of meeting KASSPER real-time demands
  - Processors In Memory (PIM)
  - Stream Processors
  - Tile Processors
  - PowerPC - baseline
- Develop KASSPER look-ahead scheduling kernels



# Vector Intelligent RAM (VIRAM, Berkeley)

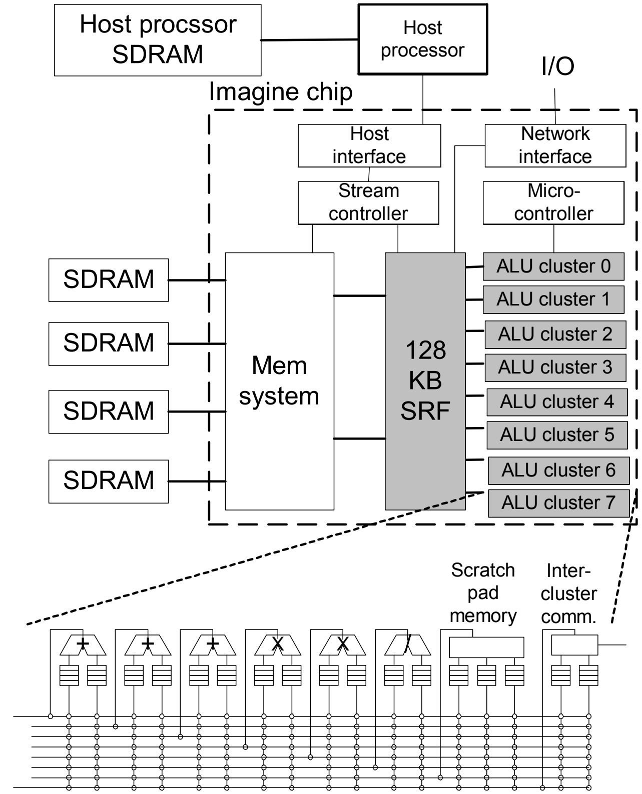
- Merge DRAM with Vector Processor
- mixed logic-DRAM CMOS process
- Scalar MIPS processor core
- 6.4 16-bit GOPS, 1.6 GFLOPS
  - 4 float ALUs; 8 32bit int ALUs; 16 16bit ALUs
- 12.8 GB/s peak memory access
- 13 MB DRAM
- 15 x 18 mm; IBM Foundry
- Chips fabbed in Q1 ‘03, ISI board on schedule for June
- C/C++ w/ pragmas, ASM; Cray PDGCS compiler
- Can add additional external DRAM
- http://iram.cs.berkeley.edu/



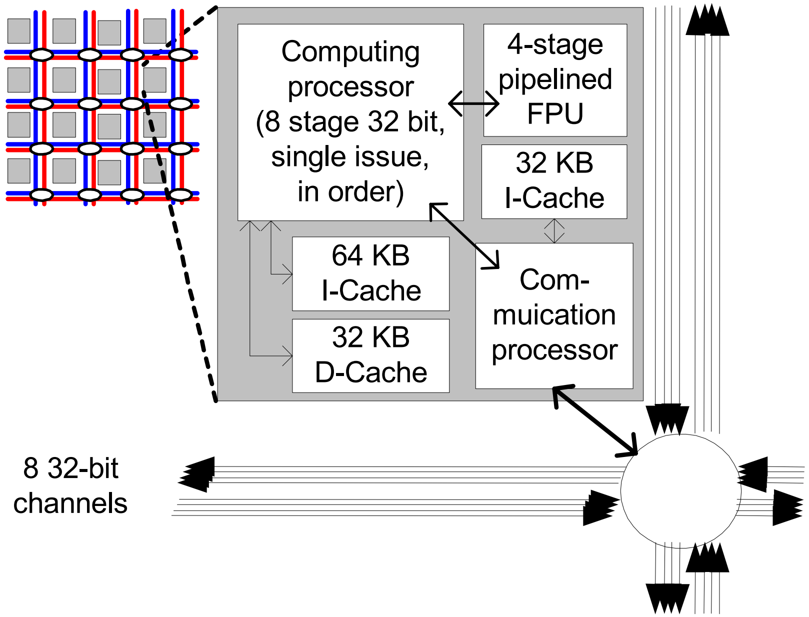
# Imagine Streaming Processor (Stanford)

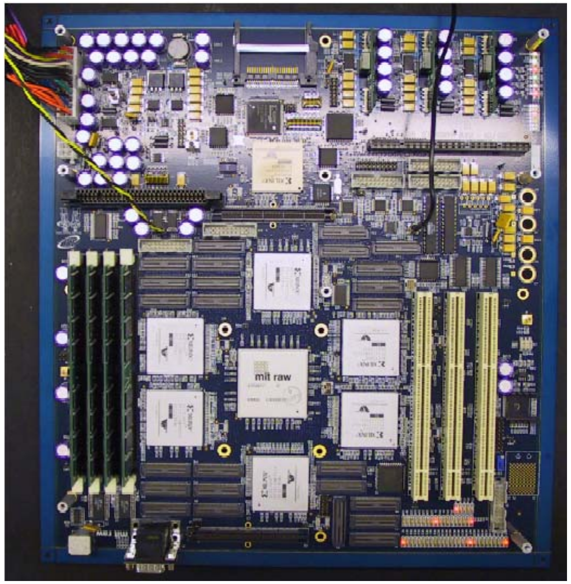
- 300 MHz, VLIW SIMD machine
- 28 16-bit GOPS, 14 GFLOPS
- 128 kB Streaming Register File
- 8 ALU Clusters
  - 6 ALUs / cluster
  - 84-95% ALU utilization typical
  - 256 x 32 bit local register file
- Streaming Memory Buffers
  - re-order DRAM accesses
  - expose data locality
  - ALU Intra-cluster BW - 435 GB/sec
  - DRAM BW - 2.1 GB/sec
- 16 x 16 mm; TI Foundry
- StreamC & KernelC programming languages
- Network interface for scalability
- Chip and board functional; Verifying benchmarks
- http://cva.stanford.edu/




# Raw (MIT)

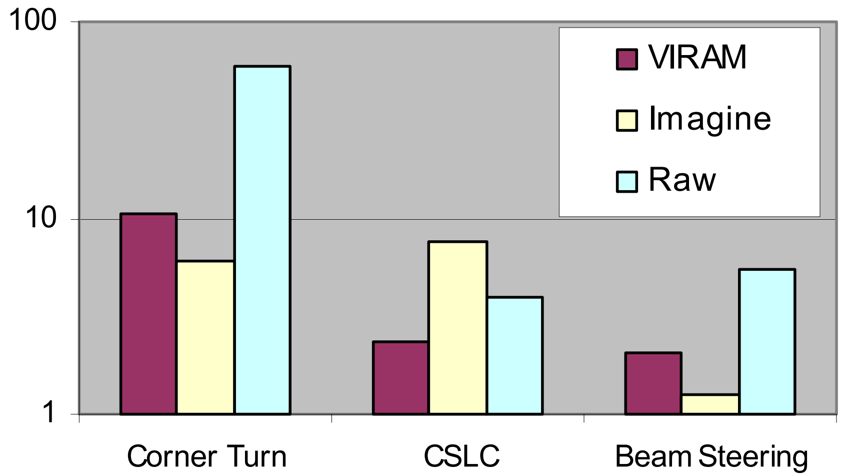
- 16 tiles of MIPS R4000 @ 300 MHz
  - 4.6 GOPS or GFLOPS
- 4 Communication Networks
  - 2 Static Networks,
    - 1 cycle throughput
    - 3 cycle latency
    - 38.3 GB / sec
  - 2 Dynamic Networks
- 14 External Ports (I/O or DRAM)
  - 33.5 GB/sec
- C and ASM; gcc based compiler
- 18.2 x 18.2 mm; IBM Foundry
- Fully scalable architecture
- Chip and board functional; Verifying benchmark performance
- http://www.cag.lcs.mit.edu/raw/



# Preliminary Benchmarks

- Benchmarks provided by LM NE&SS
- Corner Turn
  - Memory Data Movement
- Coherent Sidelobe Canceller (CSLC)
  - FFT -> Apply Weight -> IFFT
- Beam Steering
  - High Data Parallelism, Large Calibration Lookup Tables




**Speedup of execution time compared to PowerPC with Altivec**

| | PPC G4 | VIRAM | Imagine | Raw |
|---|---|---|---|---|
| Clock (MHz) | 1000 | 200 | 300 | 300 |
| # of ALUs | 4 | 16 | 48 | 16 |
| Peak GFLOPS | 5 | 3.2 | 14.4 | 4.64 |

- University chips are one silicon generation behind commercial PPC

# Summary

- PIM, Stream Processors, and Tile based Processors have shown significant gains over traditional processors in high memory BW kernels
- KASSPER systems stress memory accesses in new way
- Trade off analysis of database look-ahead scheduling time versus STAP processor throughput